Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-17 (Cancelled)

18. (New) Method of addressing a plurality of microsystems which can be individually addressed by a control circuit, the control circuit and each microsystem comprising electromagnetic transmission means, each microsystem comprising a counter and having an addressing code, an addressing phase of the microsystems comprising transmission, by the control circuit, of successive increment signals, each microsystem monitoring resetting of its counter and, upon receipt of an increment signal, incrementation of the content of its counter, and each microsystem comparing the content of its counter and its addressing code, so as to trigger execution of a pre-determined command when the content of its counter and its addressing code are identical, method wherein, the microsystems forming an array of microsystems, each microsystem comprises an identification code, in a read-only memory, and the method comprises an initialization phase successively comprising, for each microsystem, addressing, by the control circuit, of the microsystem by its identification code and storing of a reduced addressing code supplied by the control circuit in a register of the microsystem.

19. (New) Method of addressing according to claim 18, wherein the reduced addressing code of a microsystem is a function of its position in the array.

20. (New) Method of addressing according to claim 18, wherein the reduced addressing codes of the microsystems correspond to increasing numbers starting from a first microsystem.

21. (New) Method of addressing according to claim 18, wherein the microsystems are arranged in lines and columns, the reduced addressing code of each microsystem comprising a line number and a column number respectively stored in line and column registers of the microsystem, the contents of the line and column registers being respectively compared with the contents of the line and column counters of the microsystem.

22. (New) Method of addressing according to claim 21, wherein the control circuit successively transmits line increment signals and column increment signals, the line increment signals causing the content of the line counters to be incremented and the column increment signals causing the content of the column counters to be incremented and the line counters of all the microsystems to be reset.

23. (New) Method of addressing according to claim 22, wherein the microsystems are arranged in lines, in columns and according to height, the reduced addressing code comprising an additional number associated to the height, stored in an additional register associated to the height, each microsystem comprising an additional counter associated to the height, the content of the register associated to the height being compared with the content of the counter associated to the height.

24. (New) Method of addressing according to claim 23, wherein the control circuit transmits height increment signals causing the additional counters associated to the height to be incremented and the line and column counters of all the microsystems to be reset.

25. (New) Method of addressing according to claim 18, wherein a microsystem transmits an acquit signal after the latter has executed its command.

26. (New) Method of addressing according to claim 18, wherein the control circuit transmits data representative of the type of command to be executed by the microsystems in association with transmission of a reset signal.

27. (New) Method of addressing according to claim 18, wherein the control circuit transmits data representative of the type of command to be executed by the microsystems in association with transmission of an increment signal.